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POTOMAC PATENT GROUP PLLC
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EXAMINER	
RIYAMI, ABDULLA A	

ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
03/19/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,343	SPENCER, ANTHONY	
	Examiner	Art Unit	
	ABDULLAH RIYAMI	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _10 December 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-16_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-16_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to an amendment/response filed on 12/10/2008.

2. Claims 1-2 and 9-10 have been amended.

3. No claim has been canceled. No claim has been added.

4. Claims 1-16 remain pending in the application.

Response to Arguments

5. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-4, 6-12 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mittal et al. US 7035212 B1) in view of Beshai et al. (US 2004/0213291).

As per claim 1, Mittal discloses a method of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20), the method comprising:

generating from each said data packet a record portion of predetermined fixed size and containing information about the packet (see column 2, lines 39-45, ingress memory hub sends flow id and packet size to the manager, see column 2, line 16, ingress flow id is inserted in packet headers by source port, see column 2, lines 52-56, ingress flow id scheduled by traffic manager and the ingress memory hub 18 uses the pointers in the associated queue to read next packet);

storing only data portions of said packets in independent memory locations in a first memory (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id);

storing only said record portions in one or more managed queues in a second memory having fixed size memory locations equal in size to the size of the record portions (see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received);

and the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

Mittal does not expressly disclose the first memory is larger than the second memory.

Beshai discloses the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array).

Mittal and Beshai are analogous art since they are from the same field of endeavor of memory allocation for packets.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array) in Mittal's method and apparatus of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20).

The motivation to combine being to have a method and apparatus for segmenting variable size packets of a data stream in order to simplify network design and increase transport efficiency while observing delay constraints to ensure high performance (see paragraph 2, lines 3-6, Beshai).

As per claim 2, Beshai discloses wherein there are two sizes of memory location in the first memory arranged in two said blocks (see figure 9 memory a and b, see paragraph 52, lines 1-10, storage of a packet in an array of memories), one of a size to receive data portions of a first size and the other of a size to receive data portions of a second size (see figure 3, memory array, see paragraph 53, lines 1-12, packets a b and c storage arrangements a segment formed by row 312 contains data from a single packet while row 314 contains data from two or more packets), the second size being larger than the first size (see figure 3, memory array, see paragraph 53, lines 1-12,

packets a b and c storage arrangements a segment formed by row 312 contains data from a single packet while row 314 contains data from two or more packets), and wherein data portions that are too large to be stored in a single memory block are stored as linked lists in a plurality of blocks with pointers pointing to the next block (see paragraph 90, index for linked list structure of array).

As per claim 3, Mittal discloses wherein the sizes of the memory locations in the blocks are matched to the most commonly occurring sizes of data packets in the communication system (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

As per claim 4, Mittal discloses further comprising allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories).

As per claim 6, Mittal reading the data portions from the first memory in pipelined manner by a data retrieval unit adapted to instruct a memory block to read out a data portion without having to wait for the previous read to be completed, and releasing the

address location from the first memory (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

As per claim 7, Mittal discloses where there is insufficient memory for a received packet (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories, enqueueing the record portion as though the corresponding data portion was stored in the first memory(see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories, subsequently reading out the record portion corresponding to the said data packet (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories, setting a flag to indicate that the data portion of the said packet is to be discarded, discarding the said data portion, and releasing the memory location notionally allocated to the discarded data portion (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories.

Note: the functions following the phrase "adapted to" recited in claim 6, is not considered as positive limitation, i.e. the claim do not require such limitation but only require the ability to perform such functions. Therefore, it is suggested that the applicant remove the phrase "capable of" to receive full patentable weight for the subsequent limitations.

As per claim 8, Mittal discloses a bitmap of address locations and means operable such that, when a memory location is released after the data stored therein has been read out, the address of the released memory location is sent directly to the pool (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

As per claim 9, Mittal discloses a memory hub for queuing received data packets (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20), comprising:

an arrivals block, adapted to generate from each said data packet a record portion of predetermined fixed size and containing information about the packet (see column 2, lines 39-45, ingress memory hub sends flow id and packet size to the manager, see column 2, line 16, ingress flow id is inserted in packet headers by source

port, see column 2, lines 52-56, ingress flow id scheduled by traffic manager and the ingress memory hub 18 uses the pointers in the associated queue to read next packet);

a first memory for storing only data portions of said packets in independent memory locations (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id),

a second memory for storing only said record portions in one or more managed queues (see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42), the memory having fixed size memory locations equal in size to the size of the record portions (see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received);

and the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks

the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

Mittal does not expressly disclose the first memory is larger than the second memory.

Beshai discloses the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array).

Mittal and Beshai are analogous art since they are from the same field of endeavor of memory allocation for packets.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array) in Mittal's method and apparatus of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20).

The motivation to combine being to have a method and apparatus for segmenting variable size packets of a data stream in order to simplify network design and increase transport efficiency while observing delay constraints to ensure high performance (see paragraph 2, lines 3-6, Beshai).

Note: the functions following the phrase "adapted to" recited in claim 9, is not considered as positive limitation, i.e. the claim do not require such limitation but only require the ability to perform such functions. Therefore, it is suggested that the applicant remove the phrase "capable of" to receive full patentable weight for the subsequent limitations.

As per claim 10, Beshai discloses wherein there are two sizes of memory location in the first memory arranged in two said blocks (see figure 9 memory a and b, see paragraph 52, lines 1-10, storage of a packet in an array of memories), one of a size to receive data portions of a first size and the other of a size to receive data portions of a second size (see figure 3, memory array, see paragraph 53, lines 1-12, packets a b and c storage arrangements a segment formed by row 312 contains data from a single packet while row 314 contains data from two or more packets), the second size being larger than the first size (see figure 3, memory array, see paragraph 53, lines 1-12, packets a b and c storage arrangements a segment formed by row 312 contains data from a single packet while row 314 contains data from two or more packets), and wherein data portions that are too large to be stored in a single memory block are stored as linked lists in a plurality of blocks with pointers pointing to the next block but without any pointers pointing from one data portion to the next data portion of the packet (see paragraph 90, index for linked list structure of array).

As per claim 11, Mittal wherein the sizes of the memory locations in the blocks are matched to the most commonly occurring sizes of data packets in the communication system (see figure 2, ingress memory 20, see column 4, lines 31-40, the

ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

As per claim 12, Mittal discloses allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories).

As per claim 14, Mittal discloses a data retrieval unit adapted to read out the data portions from the first memory in pipelined manner and to instruct a memory block to read out a data portion without having to wait for the previous read to be completed, and releasing the address location from the first memory (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

Note: the functions following the phrase "adapted to" recited in claim 6, is not considered as positive limitation, i.e. the claim do not require such limitation but only require the ability to perform such functions. Therefore, it is suggested that the applicant remove the phrase "capable of" to receive full patentable weight for the subsequent limitations.

As per claim 15, Mittal discloses where there is insufficient memory for a received packet (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories), enqueueing the record portion as though the corresponding data portion was stored in the first memory(see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories), subsequently reading out the record portion corresponding to the said data packet (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories), setting a flag to indicate that the data portion of the said packet is to be discarded, discarding the said data portion, and releasing the memory location notionally allocated to the discarded data portion (see column 4, lines 31-40, writes packet according to flow id and threshold (see column 5, 15-20), see column 7, lines 36-65, allocating and addressing ingress packets in memories).

As per claim 16, Mittal discloses a bitmap of address locations and means operable such that, when a memory location is released after the data stored therein

has been read out, the address of the released memory location is sent directly to the pool (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received).

10. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mittal et al. US 7035212 B1) in view of Beshai et al. (US 2004/0213291) further in view of Radharkrishnan et al. (US 2004/0022094 A1).

As per claim 5, Mittal discloses a method of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20) and Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array). Mittal and Beshai do not expressly disclose the memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels.

Radharkrishnan discloses the memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (see paragraph 31, Scalable Node Controller (SNC) 110A and the I/O Hub (IOH) 120A, the SNC 110A may support one to four processors 100A and may interface directly or substantially directly to the processor's Bus 105A, the main memory controller in the SNC 110A may support four memory channels, a double data rate (DDR) memory hub(DMH) on each memory channel may control eight DDR dual in-line memory modules(DIMM)).

Radharkrishnan, Mittal and Beshai are analogous art since they are from the same field of endeavor of memory allocation for packets.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Radharkrishnan's technique of using memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (see paragraph 31, Scalable Node Controller (SNC) 110A and the I/O Hub (IOH) 120A, the SNC 110A may support one to four processors 100A and may interface directly or substantially directly to the processor's Bus 105A, the main memory controller in the SNC 110A may support four memory channels, a double data rate (DDR) memory hub(DMH) on each memory channel may control eight DDR dual in-line memory modules(DIMM)) in Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see

paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array) in Mittal's method and apparatus of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20).

The motivation to combine being to have a method and apparatus for addressing needs of different server segments to address the needs for low-end systems and design proprietary components for mid-range and high-end systems (see paragraph 5, lines 10-15, Radharkrishnan).

As per claim 13, Mittal discloses a method of queuing variable size data packets in a communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20) and Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array). Mittal and Beshai do not expressly disclose the memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels.

Radharkrishnan discloses the memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (see

paragraph 31, Scalable Node Controller (SNC) 110A and the I/O Hub (IOH) 120A, the SNC 110A may support one to four processors 100A and may interface directly or substantially directly to the processor's Bus 105A, the main memory controller in the SNC 110A may support four memory channels, a double data rate (DDR) memory hub(DMH) on each memory channel may control eight DDR dual in-line memory modules(DIMM)).

Radharkrishnan, Mittal and Beshai are analogous art since they are from the same field of endeavor of memory allocation for packets.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Radharkrishnan's technique of using memory blocks are segregated into a plurality of memory channels and allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (see paragraph 31, Scalable Node Controller (SNC) 110A and the I/O Hub (IOH) 120A, the SNC 110A may support one to four processors 100A and may interface directly or substantially directly to the processor's Bus 105A, the main memory controller in the SNC 110A may support four memory channels, a double data rate (DDR) memory hub(DMH) on each memory channel may control eight DDR dual in-line memory modules(DIMM)) in Beshai's technique of using memories wherein the first memory is larger than the second memory (see figure 9 memory B is larger that memory C, see paragraph 87 lines 1-30, memory C has stored control data while memory B has data stored of the streams, see paragraph 90, index for linked list structure of array) in Mittal's method and apparatus of queuing variable size data packets in a

communication system (see figure 1a, end to end forwarding architecture, ingress memory hub 18, ingress memory 20).

The motivation to combine being to have a method and apparatus for addressing needs of different server segments to address the needs for low-end systems and design proprietary components for mid-range and high-end systems (see paragraph 5, lines 10-15, Radharkrishnan).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2416

/Abdullah Riyami/
Examiner, Art Unit 2416